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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,897	10/30/2003	Harm Peter Hofstee	AUS920030402US1	9220

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IBM CORPORATION- AUSTIN (JVL)
C/O VAN LEEUWEN & VAN LEEUWEN
PO BOX 90609
AUSTIN, TX 78709-0609

EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	

MAIL DATE	DELIVERY MODE
05/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,897	HOFSTEE ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *2, 9-10, 12, 14, 19, and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,11,13,15-18,20 and 22-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The present Office Action is taken in response to applicant's communication filed February 27, 2007 responding to Non-Final rejection dated November 30, 2006 and Interview dated February 16, 2007. Applicant's amendments and/or arguments have been considered with the results that follow.

2. Claims 1, 3-8, 11, 13, 15-18, 20, 22-30 are now pending in the application under prosecution as claims 2, 9-10, 12, 14, 19, and 21 were canceled by applicant's amendment.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 3-8, 11, 13, 15-18, 20, and 22-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 3-8, 11, 13, 15-18, 20, and 22-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,601,146 (Auslander et al) in view of (US 6,813,522 (Schwarm et al).

With respect to claims 1 and 25, Auslander discloses the invention as claimed, a memory shared by a plurality of heterogeneous processors *[(a shared memory computer system having more than two processes and a plurality of processors, including a client processor and a server processor) Fig. 1-2; Col. 8, Lines 41-43]* comprising: the shared memory, wherein the shared memory accessible by one or processors adapted process a first instruction set; wherein the shared memory accessible by one of second processors that are adapted to process a second instruction set *[(plurality of processes on respective & specific processor including client and server [Fig. 2; Col. 4, Lines 15-19]*; a memory map corresponding to the shared memory, wherein the memory map includes cross-references between virtual addresses and real addresses, the memory map and the cross-references shared between the first processors and the second processors *[(a map mapping a single, undivided fixed interprocess communication transfer region having a unique physical address at said shared memory to each of a plurality of virtual addresses, i.e., the system maps a common piece of physical memory into a process's virtual address space) Col. 2, Line 58 to Col. 3, Line 2; Col. 3, Lines 54-61].* Applicant argues that

Auslander fails to teach a single memory map to include cross-references shared between the first processor and the second processor. However, Schwarm teaches multiprocessor system permitting each processor to run concurrently separate invocations of a program (i.e. each program adapted to process separate instruction sets), and each processor uses the same address translation for shared access to the program code in a shared memory (Abstract; Col. 2, Lines 40-57; Col. 3, Lines 7-17]. Therefore it would have been obvious to one having ordinary skill in the art and having both teachings before him at the time of the invention to have a single memory map to include cross-references shared between the first processor and the second processor because Schwarm teaches multiprocessor system where each processor uses the same address translation for shared access to a program code in a shared memory area. The combination is proper because mapping to the shared memory using a single translation would have permitted read-only accesses by all processor in the system and, therefore, improved the system performance by eliminating the restrictions of operating system functions previously restricted to a single processor.

With respect to claims 11 and 18, Auslander discloses the invention as claimed, a method for sharing a memory between a plurality of heterogeneous processors *[(a shared memory computer system having more than two processes and a plurality of processors, including a client processor and a server processor) Fig. 1-2; Col. 8, Lines 41-43]* comprising:

allocating a first memory partition on the shared memory that corresponds to a memory request, the first memory partition accessible by one or more first processors that are adapted to process a first instruction set *[(for each processors mapping plurality of virtual addresses in each address space of a common shared memory allocated to processes of each processor) Fig. 2]*;

assigning a second memory partition on the shared memory to one or more second processors that are adapted to process a second instruction set *[(for each processors mapping plurality of virtual addresses in each address space of a common shared memory allocated to processes of each processor) Fig. 2]*; wherein the first processors and the second processors are heterogeneous [Fig. 2 shows virtual address space assigned to client processes and virtual address space assigned to server processes];

managing the first memory partition and the second memory partition using a common memory map wherein the common memory map includes a plurality regions selected from a group consisting of an external system memory, local storage alias region, a TLB region, operating system region, and I/O device region [Physical memory region, Fig. 1 & 2; Col. 4, Lines 29-38];

wherein the TLB region includes cross-references between virtual addresses and real addresses, the memory map and the cross-references shared between the first processors and the second processors *[(a map mapping a single, undivided fixed interprocess communication transfer region having a unique physical address at said shared memory to each of a plurality of virtual addresses, i.e., the system maps a*

common piece of physical memory into a process's virtual address space) Col. 2, Line 58 to Col. 3, Line 2; Col. 3, Lines 54-61; Col. 4, Lines 29-38].

Applicant argues that Auslander fails to teach a single memory map to include cross-references shared between the first processor and the second processor. However, Schwarm teaches multiprocessor system permitting each processor to run concurrently separate invocations of a program (i.e. each program adapted to process separate instruction sets), and each processor uses the same address translation for shared access to the program code in a shared memory (Abstract; Col. 2, Lines 40-57; Col. 3, Lines 7-17]. Therefore it would have been obvious to one having ordinary skill in the art and having both teachings before him at the time of the invention to have a single memory map to include cross-references shared between the first processor and the second processor because Schwarm teaches multiprocessor system where each processor uses the same address translation for shared access to a program code in a shared memory area. The combination is proper because mapping to the shared memory using a single translation would have permitted read-only accesses by all processor in the system and, therefore, improved the system performance by eliminating the restrictions of operating system functions previously restricted to a single processor.

With respect to claims 3-8, 13, 15-17, 20, 22-30, Auslander teaches as claimed, an operating system operating on the processors that controls the memory map; local storage and memory management unit including memory controller; the storage being

divided into private storage and non-private storage [fig. 2; Col. 4, Lines 26-38; Co. 6, Lines 13-23]; Schwarm additionally teaches multiple processors to perform different functions for a shared program and a desirable need to have a single invocation of a program control a low-level function, such as a device driver for an input/output device that is to be shared among the processors; the multiprocessor system including a boot processor 21 and a clone processors 22, 23 executing a shared program 31, each of the processors 21, 22, 23 running a separate respective invocation of the shared program 31, each invocation producing a different set of data during read-write access to the shared memory 25, each of the processors having a respective address translator 32, 33, 34 that permits the respective processors to execute the same read-write access instructions in the shared program for accessing respective different regions of the shared memory. (See Col. 5, Lines 15-57; Col. 6, Lines 38-53.)

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon, Tue-Fri (8:00A to 5:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186